

**In The Claims**

Applicant submits below a complete listing of the current claims, with any insertions indicated by underlining and any deletions indicated by strikeouts and/or double bracketing.

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of the Claims**

1. (Currently amended) 0A monitoring device (~~18', 18"~~) integrated ~~to~~ on the chip of a microprocessor (~~12~~) executing a sequence of instructions, comprising:

a message calculation means (~~36~~) for, on each execution of an instruction from among a plurality of instructions of predetermined types, generating a digital message corresponding to the executed instruction;

a buffer memory (~~34~~) for storing each generated message; and

a plurality of output terminals (~~FA, FB, FC~~) connected to an external analysis tool (~~24~~), each output terminal (~~FA, FB, FC~~) being associated with one of the instruction types and the message calculation means (~~36~~) modifying the state of the output terminal (~~FA, FB, FC~~) associated with an instruction type at the time when a message corresponding to said instruction type is stored in the buffer memory.

2. (Currently amended) The monitoring device (~~18', 18"~~) of claim 1, wherein the buffer memory is divided into several areas (~~A, B, C~~), each of which is associated with a different instruction type and is intended to only store messages associated with said instruction type.

3. (Currently amended) The monitoring device of claim 1, wherein each output terminal (~~FA, FB, FC~~) is connected to a test terminal (~~28, 30, 32~~).

4. (Currently amended) The monitoring device of claim 1, wherein each output terminal (~~FA, FB, FC~~) is connected to an input terminal (~~F~~) of a coding block (~~38, 40, 42~~) comprising a predetermined number (~~n~~) of output terminals (~~O1, O2, O3~~), each of which is

connected to a test terminal (281, 282, 283; 301, 302, 303; 321, 322, 323); each coding block being provided to have each of its n output terminals ( $O_1, O_2, O_3$ ) switch once every n state switchings of its input terminal ( $F$ ) and so that a single one of its n output terminals ( $O_1, O_2, O_3$ ) switches state at once.

5. (Currently amended) The monitoring device of claim 1, wherein certain types of instructions only are associated with an output terminal of the message calculation means (24).

6. (Currently amended) The monitoring device of claim 1, wherein each of the possible instruction types is associated with an output terminal ( $FA, FB, FC$ ) of the message calculation means (24).

7. (Currently amended) An integrated circuit (10) comprising a microprocessor (12) and the monitoring device of claim 1.

8. (Currently amended) A method for monitoring a microprocessor (12) executing a sequence of instructions by means of a device integrated to the microprocessor chip, comprising the steps of:

on each execution of an instruction, generating a digital message corresponding to the executed instruction; and

storing each generated message in a buffer memory (34); and

modifying the state of one of a plurality of output terminals ( $FA, FB, FC$ ) connected to an external analysis tool (24) and each associated with an instruction type when a message corresponding to the instruction type to which said output terminal is associated is stored in the buffer memory.